



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,219	09/26/2003	Naotaka Yumoto	030712-14	6834
22204	7590	09/07/2005	EXAMINER	
NIXON PEABODY, LLP 401 9TH STREET, NW SUITE 900 WASHINGTON, DC 20004-2128			HUR, JUNG H	
			ART UNIT	PAPER NUMBER
			2824	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/670,219

Applicant(s)

YUMOTO, NAOTAKA

Examiner

Jung (John) Hur

Art Unit

2824

— The MAILING DATE of this communication appears on the cover sheet with the correspondence address —
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 June 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) 6-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 21-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Amendment

1. Acknowledgment is made of applicant's Amendment, filed 23 June 2005. The changes and remarks disclosed therein have been considered.

No claims have been cancelled or added by the Amendment. Therefore, claims 1-29 are pending in the application.

Election/Restrictions

2. Claims 6-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11 February 2005. The Restriction requirement is made final.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 3-5, 21, 23-26, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art ("Admission") in view of McClure (U.S. Pat. No. 6,037,792).

Admission (for example, in the second paragraph on page 1) discloses a nonvolatile semiconductor memory device comprising: a memory cell array having a plurality of memory cells and arranged in an array, the memory cells being connected to a plurality of bit lines and word lines (inherent); a plurality of address input terminals inputting a plurality of addresses thereto (inherent); a test mode circuit for outputting a test mode signal (implied, for example, to control the selection of all word lines) when a signal ("a signal from the exterior") is inputted to a predetermined terminal (implied, since the signal is from the exterior); a row decoder connected to said test mode circuit (implied, since all word lines are selected for testing) and applying an excess voltage ("a test mode voltage" of 8V, above the normal level of 5V) for a test to all said word lines in response to said test mode signal; a column decoder (including "column switches") connected to said test mode circuit and setting all said bit lines to a non-selecting state ("a turning-off state") in response to said test mode signal; a control signal input terminal for receiving a control signal (inherent; such as RAS, CAS, R/W, etc.) and a control circuit connected to this control signal input terminal (inherent, for example, to control read/write operations); and an address buffer connected to the address input terminals, the row decoder and the column decoder (inherent).

However, Admission does not disclose that the predetermined terminal is that among the address input terminals; and a monitor terminal (or pad) connected to said test mode circuit and outputting said test mode signal.

McClure, for example in Fig. 1, discloses outputting a test mode signal (for example, /BURN-IN MODE signal) when a signal is inputted to a predetermined terminal among the address input terminals (i.e., use of an address pin to control entry into the test mode; see, for

Art Unit: 2824

example, column 5, lines 52-61). McClure further discloses a monitor terminal or pad (48 or 54) for outputting the test mode signal (via 52 and 50; see also column 3, lines 22-40 and column 5, lines 37-52).

Since it was common and well known in the art to detect a predetermined signal on an existing address pin to enable a test mode (as exemplified by McClure and others), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to enable the test mode of Admission via a signal on a predetermined terminal among the address input terminals, for the purpose of reducing the need for additional pins to enable a test mode and thus reducing the space and cost associated with providing additional pins.

Further, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate a test mode monitor terminal (or pad), as in McClure, in the test mode circuit of Admission, for the purpose of ascertaining a test mode entry and exit and thus reducing test errors and increasing test quality (see also for example McClure, column 5, lines 40-44).

5. Claims 2, 22 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art ("Admission") in view of McClure (U.S. Pat. No. 6,037,792) as applied to claims 1, 21 and 26 above, and further in view of Fontana et al. (U.S. Pat. No. 5,982,677).

The above Admission/McClure combination disclose a memory device as in claims 1, 21 and 26 above, with the exception of a select line connected to the drain of a memory cell, and a regulator connected to this select line and said test mode circuit and giving a predetermined bias electric potential to the drain of said memory cell.

Fontana, for example in Figs. 2 and 3, discloses a select line (Yms) connected to the drain of a memory cell (see 3 in Fig. 2), and a regulator (Fig. 3) connected to this select line and a circuit (providing Vref and PGn), and giving a predetermined bias electric potential to the drain of said memory cell (see for example column 4, lines 26-37).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the drain voltage regulator, as in Fontana, in the device of the Admission/McClure combination, such that the regulator would be connected to the test mode circuit and provide a test voltage to the drains of the memory cells, for the purpose of stabilizing the test voltage and reducing the testing time, and thus improving the test efficiency (see for example Fontana, column 3, lines 37-46; also, column 7, lines 24-28).

Response to Arguments

6. Applicant's arguments filed 23 June 2005 have been fully considered but they are not persuasive.

Regarding claims 1, 21 and 26, Applicant argues, starting in the middle of the last paragraph on page 11, that "McClure discloses a semiconductor memory device having a flag terminal for outputting a burn-in stress test signal. The burn-in stress test is conducted at significantly higher voltages and temperature conditions in order accelerate weak bit failures and infant life failures as noted in column 3, lines 7-10. Furthermore, the burn-in stress test is conducted in a burn-in oven as noted from the Abstract. Accordingly, the flag terminal of McClure is used for confirming whether the device is in the burn-in stress mode or not. Clearly,

Art Unit: 2824

the flag pad of McClure and the monitoring pad of the present invention are significantly different.”

In response, it is noted that, in McClure, the burn-in mode is a test mode, and the /BURN-IN MODE signal in Fig. 1 is a test mode signal; thus, terminals 48 and 54 in Fig. 1 of McClure are monitor terminals outputting a test mode signal (via 50 and 52). Therefore, although the nature or the type of tests is different between the admitted prior art and McClure, one of ordinary skill in the art would find the monitor terminals of McClure to be applicable and useful in the device of the admitted prior art, for the purpose cited in the previous rejection and repeated above.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Art Unit: 2824

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870.

The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh



**ANH PHUNG
PRIMARY EXAMINER**